Lecture 12 Network Computing II Interconnection Networks, Grid

Ceng505 Parallel Computing at December 27, 2010

Network Computing I Dr. Cem Özdoğan

Interconnection Networks Ethernet Switches Myrinet Clos Network The Quadrics Network

Grid Computing

Dr. Cem Özdoğan Computer Engineering Department Çankaya University

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Interconnection Networks

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- Multiple machines can access an Ethernet at the same time.
- Each machine senses whether a carrier wave is present to determine whether the network is <u>idle</u> before it sends a packet.
- Only when the network is not busy sending another message can transmission start.

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• Each transmission is limited in duration and there is a minimum idle time between two consecutive transmissions by the same sender.



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- The network configuration of a high-performance cluster is dependent on
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 - the price for each of the components.

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Interconnection Networks

Ethernet

Switches

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- The case of <u>many-to-one</u> should cause conflicts at the output ports and therefore needs arbitration to resolve conflicts if allowed.
- When only one-to-one connections are allowed, the switch is called <u>crossbar</u>.

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• An *n* × *n* crossbar switch can establish *n*! connections (to allow only one-to-one connections,

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 - Thus, the number of one-to-one connections is $n * (n 1) * (n 2) \dots * 2 * 1 = n!$



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Interconnection Networks Ethernet

Switches

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- For example, a binary switch has two input(output) ports.



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- For example, a binary switch has two input(output) ports.
- The number of one-to-one connections in a binary switch is two (straight and crossed),
- while the number of all allowed connections is four (straight, crosses, lower broadcast, and upper broadcast).



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• Routing can be achieved using two mechanisms:



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- Routing can be achieved using two mechanisms:
- 1 **Source-path**, the entire path to the destination is stored in the packet header at the source location.

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- Routing can be achieved using two mechanisms:
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- When a packet enters the switch, the outgoing port is determined from the <u>header</u>.



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- Routing can be achieved using two mechanisms:
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- Used routing data is stripped from the header and routing information for the next switch is now in the front.



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- 2 **Table-based routing**, the switch must have a complete routing table that determines the corresponding port for each destination.

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- When a packet enters the switch, a table lookup will determine the outgoing port.

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Switches IV

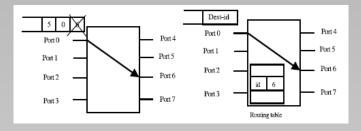


Figure: Source-path routing vs. table-based routing.

• Figure 1 illustrates the difference between source-path routing and table-based routing in the case when a packet enters an 8-port switch at port 0.

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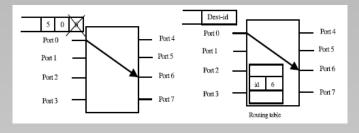


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Switches IV

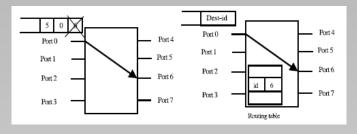


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- In the source-path case, the header contains the entire path and the next port is port 6.
- In the table-based case, the destination address dest-id is looked up in the routing table and port 6 is followed.

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- Myrinet switches are <u>multiple-port</u> (4, 8, 12, 16) components that route a packet entering on an input channel of a port to the output channel of the port selected by the packet.

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- For an *n*-port switch, the ports are addressed 0, 1, 2, ..., *n* − 1.
- For any switching permutation, there may be as many packets traversing a switch concurrently as the switch has ports.

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• These switches are implemented using two types of chips:

crossbar-switch chips and the Myrinet-interface chip.

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- These switches are implemented using two types of chips: crossbar-switch chips and the Myrinet-interface chip.
- The basic building block of the Myrinet-2000 network is a 16-port Myrinet crossbar switch, implemented on a single chip designated as Xbar16.

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- The basic building block of the Myrinet-2000 network is a 16-port Myrinet crossbar switch, implemented on a single chip designated as Xbar16.
- It can be interconnected to build various topologies of varying sizes.
- The most common topology is the Clos network.

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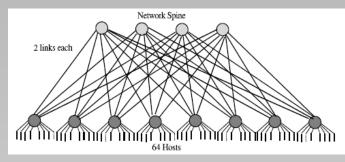


Figure: A 64-host Clos network using 16-port Myrinet switch (each line represents two links).

• A network of 64 hosts or fewer would require eight-port switches for the spine.

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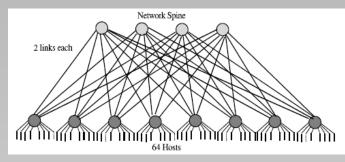


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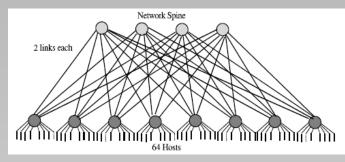


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- The thick line connecting a spine switch to a leaf switch represents two links.

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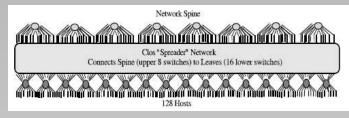


Figure: A 128-host Clos network using 16-port Myrinet switch, which includes 24 Xbar16s.

• Each Xbar16 switch is represented using a circle.

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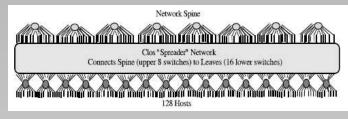


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- The eight switches forming the upper row is the Clos network *spine*, which is connected through a Clos spreader network to the 16 *leaf* switches forming the lower row.

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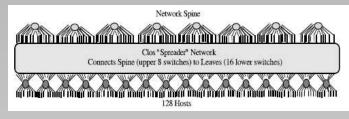


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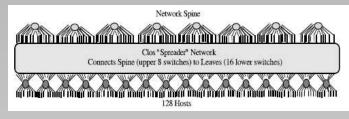


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- Routes between hosts connected to different Xbar16s traverse three Xbar16 switches.

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- The routing of Myrinet packets is based on the source routing approach.
- Each Myrinet packet has a variable length header with complete routing information.
- When a packet enters a switch, the leading byte of the header determines the outgoing port before being stripped off the packet header.

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- The routing of Myrinet packets is based on the source routing approach.
- Each Myrinet packet has a variable length header with complete routing information.
- When a packet enters a switch, the leading byte of the header determines the outgoing port before being stripped off the packet header.
- At the host interface, a control program is executed to perform source-route translation.

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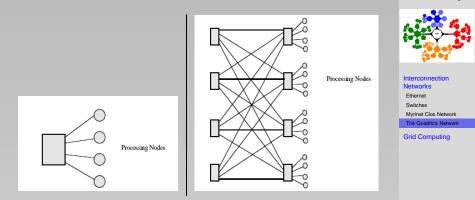


Figure: Quaternary fat tree of dimension 1 (left) and Elite switch of Quadrics networks (right).

• The Quadrics network (QsNet) consists of two hardware building blocks:

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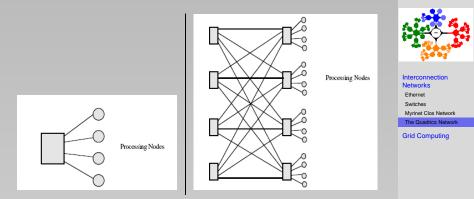


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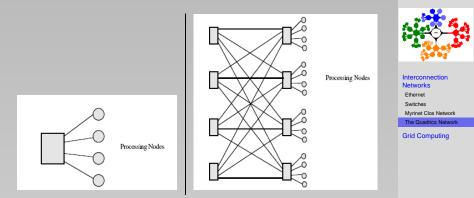


Figure: Quaternary fat tree of dimension 1 (left) and Elite switch of Quadrics networks (right).

- The Quadrics network (QsNet) consists of two hardware building blocks:
 - a programmable network interface called Elan and
 - a high-bandwidth, low-latency communication switch called Elite.

 The Elan network interface connects the Quadrics network to a processing node containing one or more CPUs.

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- The Elan network interface connects the Quadrics network to a processing node containing one or more CPUs.
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- A <u>quaternary</u> fat tree of dimension *n* is composed of 4ⁿ processing nodes and n × 4ⁿ⁻¹ switches interconnected as a delta network.

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- Figure 3left and -right shows quaternary fat trees of dimensions 1 and 2, respectively.
- When *n* = 1, the network consists of one switch and four processing nodes.
- When *n* = 2, the network consists of eight switches and 16 processing nodes.

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Interconnection Networks Ethernet Switches Myrinet Clos Network The Quadrics Network Grid Computing

• Elite networks are source routed.



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- In QsNet, the size of each flit is 16 bits. Network nodes can send packets to multiple destinations using the network's broadcast capability.

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Table: List of local area networks device bandwidths.

Interconnection	Data Rate	Data Rate	Year
Technology	(bit/s)	(byte/s)	
Ethernet (10BASE-X)	10 Mbit/s	1.25 MB/s	1990
Fast Ethernet (100BASE-X)	100 Mbit/s	12.5 MB/s	1995
FDDI	100 Mbit/s	12.5 MB/s	
Token Ring IEEE 802.5v	1 Gbit/s	125 MB/s	2001
Gigabit Ethernet (1000BASE-X)	1 Gbit/s	125 MB/s	1998
Myrinet 2000	2 Gbit/s	250 MB/s	
Infiniband SDR 1X[24]	2 Gbit/s	250 MB/s	
Quadrics QsNetl	3.6 Gbit/s	450 MB/s	
Infiniband DDR 1X[24]	4 Gbit/s	500 MB/s	
Infiniband QDR 1X[24]	8 Gbit/s	1 GB/s	
Infiniband SDR 4X[24]	8 Gbit/s	1 GB/s	

Interconnection Networks Ethernet Switches Myrinet Clos Network The Quadrics Network Grid Computing

Interconnection Networks II

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Data Rate Interconnection Data Rate Year Technology (bit/s) (byte/s) Quadrics QsNetII 8 Gbit/s 1 GB/s 10 Gigabit Ethernet (10GBASE-X) 10 Gbit/s 1.25 GB/s Myri 10G 10 Gbit/s 1.25 GB/s Infiniband DDR 4X[24] 16 Gbit/s 2 GB/sScalable Coherent Interface (SCI) Dual Channel SCI, x8 PCIe 20 Gbit/s 2.5 GB/s Infiniband SDR 12X[24] 24 Gbit/s 3 GB/s Infiniband QDR 4X[24] 32 Gbit/s 4 GB/s 40 Gigabit Ethernet (40GBASE-X) 40 Gbit/s 5 GB/s Infiniband DDR 12X[24] 48 Gbit/s 6 GB/s Infiniband QDR 12X[24] 96 Gbit/s 12 GB/s 100 Gigabit Ethernet (100GBASE-X) 12.5 GB/s 100 Gbit/s

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• While clusters are collections of computers tied together as a single system,

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Interconnection Networks Ethernet Switches Myrinet Clos Network The Quadrics Network

- While clusters are collections of computers tied together as a single system,
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- Resembling an electric power grid, the computing grid is expected to become a pervasive (spread throughout) computing infrastructure that supports <u>large-scale</u> and <u>resource-intensive</u> applications.
- The significant increase in application complexity and the need for collaboration have made grids an attractive computing infrastructure.

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• Thus, the need for the distributed grid infrastructure will continue to be an important resource.

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- and then allocating them to individual tasks as the need arise.
- Resources are returned to the pool upon completion of the task.
- Grid gives an illusion of a big virtual computer capable of carrying out enormous tasks.

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· Support of grids requires innovative solutions to a number

of challenging issues including:

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- Support of grids requires innovative solutions to a number of challenging issues including:
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 - performance.

• There are several examples of grid platforms and tools such as <u>Globus</u> and <u>TeraGrid</u>.



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 - The Globus Toolkit has grown through an open-source strategy. Version 1.0 was introduced in 1998 followed by the 2.0 release in 2002. The latest 3.0 version is based on new open-standard Grid services.

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• **TeraGrid** is a large high-performance computing project headed by the National Center for Supercomputing Applications at the University of Illinois at Urbana-Champaign.

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- These components will be tightly integrated and connected through a network that will operate at 40 gigabits per second.

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