Lecture 2

Introduction

View of the Field

Ceng505 *Parallel Computing* at October 4, 2010

Dr. Cem Özdoğan
Computer Engineering Department
Çankaya University

Contents

Field I

- Data-intensive applications;

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  - transaction processing,

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- *Multiprocessor* – Multiple processors cooperate to jointly execute a single computational task in order to speed up its execution.

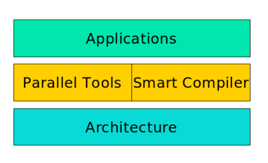
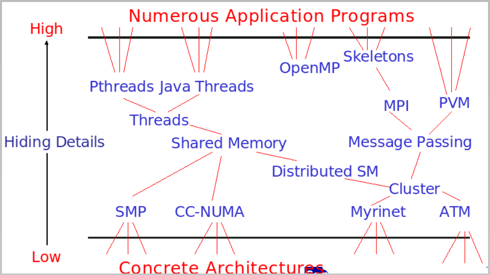


Figure: Abstraction Layers

Field III



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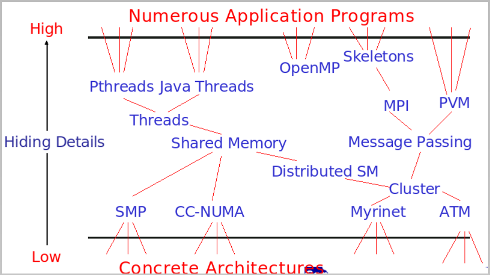

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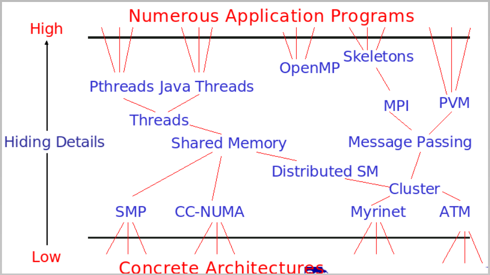

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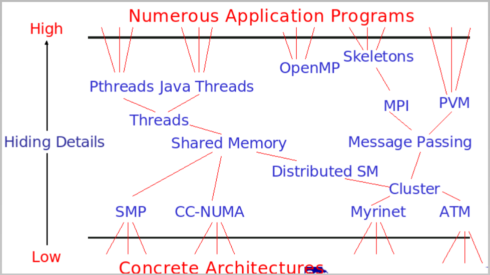

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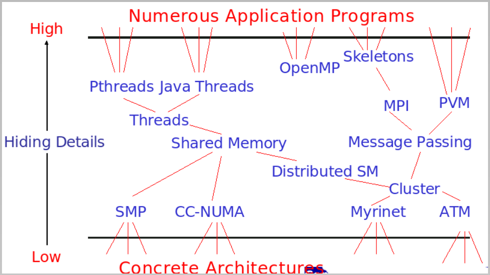

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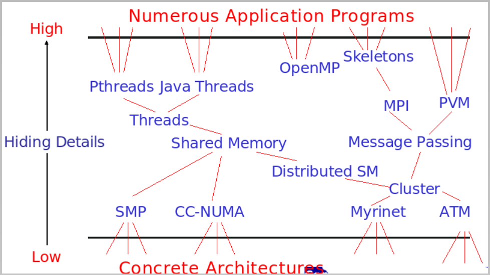

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5. Current Trends: Clusters, Grids.

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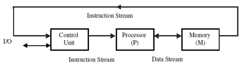

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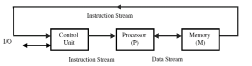

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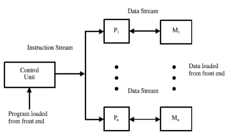

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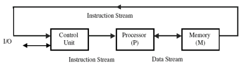

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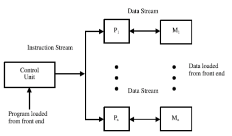

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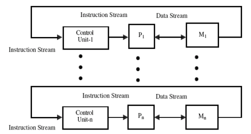

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- In a MIMD machine, each processor has its own control unit and can execute different instructions on different data.
- In the MISD category, the same stream of data flows through a linear array of processors executing different instruction streams. In practice, there is no viable MISD machine; however, some authors have considered *pipelined machines* as examples for MISD.

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- MIMD Shared Memory, MIMD Distributed Memory
- Bus based, Switch based
- CC-NUMA
- Clusters, Grid Computing
  - Grids are geographically distributed platforms for computation.

Parallel and Distributed Computers I

- The processing units can communicate and interact with each other using either
  - shared memory
  - or message passing methods.
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  - Grids are geographically distributed platforms for computation.
  - They provide dependable, consistent, general, and inexpensive access to high end computational capabilities.

Parallel and Distributed Computers II

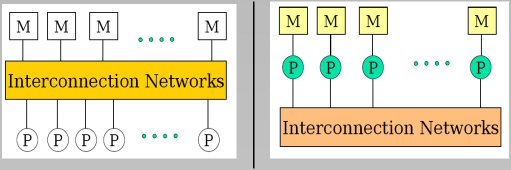

Figure: (a) MIMD Shared Memory, (b) MIMD Distributed Memory.

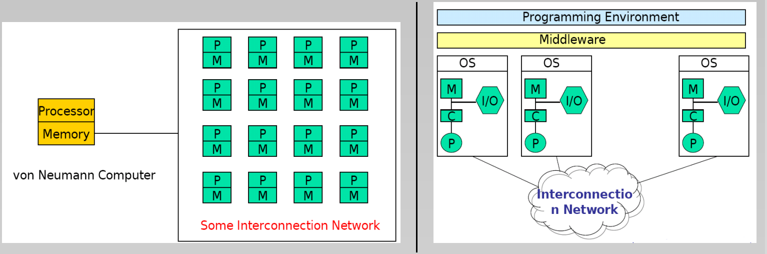

Figure: (a) SIMD Distributed Computers, (b) Clusters.

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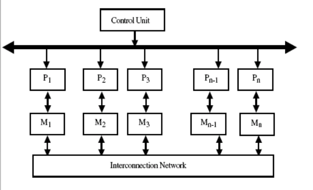
- There are two main configurations that have been used in SIMD machines (see Fig. 5).

SIMD Architecture II



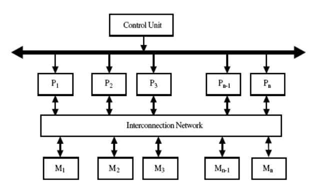


Figure: Two SIMD Schemes.

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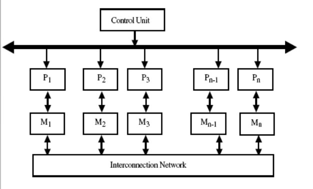

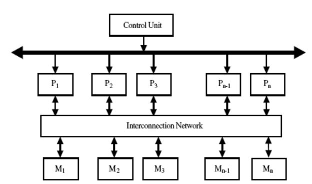

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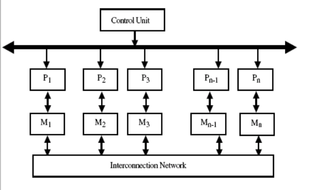

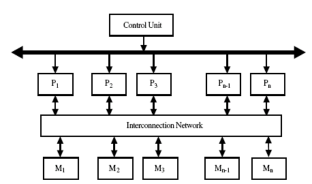

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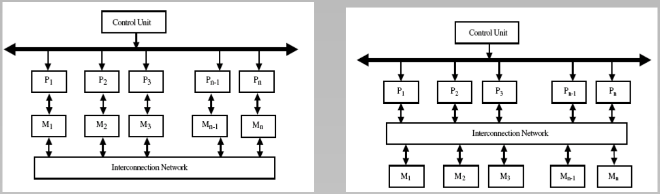

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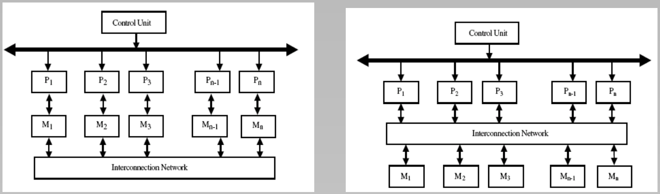

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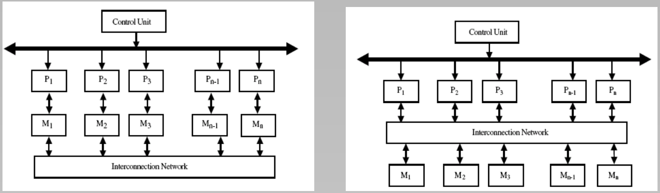

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   - Two processors can transfer data between each other via intermediate memory module(s) or possibly via intermediate processor(s).

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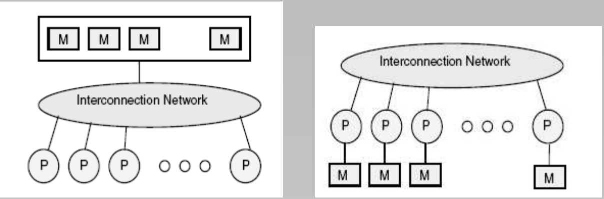

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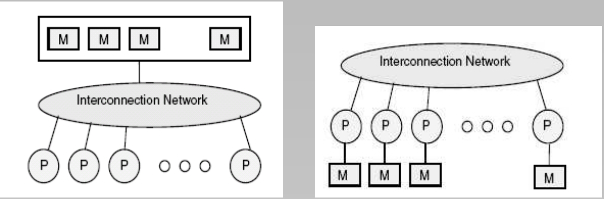

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- If scalability to larger and larger systems (as measured by the number of processors) was to continue, systems had to use distributed memory techniques.

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  - Thus, the DSM machine is a *hybrid* that takes advantage of both design schools.

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- Requests arrive at the memory module through its two ports.

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  - A COMA system requires that data be migrated to the processor requesting it.

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